

ACER_SJM31

MAIN BOARD

2009.05.04

Monday, May 04, 2009	2009-ECO-006989	A
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE	TITLE	INVENTEC			
DRAWER						ACER SJM31			
DESIGN									
CHECK									
RESPONSIBLE									
SIZE=					SIZE	CODE	DOC NUMBER		REV
FILE NAME: XXXX-XXXXXX-XX					C	CS	D-CS-1310A22752-0-ALG		B
P/N: XXXXXXXXXX					SHEET		of		36

1. Schematic Page Description :

Montevina Schematic Ver : A02

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Annotations

5. Schematic Modify

6. Timing Diagram

7. Power Block Diagram

8. Adaptor in/Charge

9. 5VLA/5VA/3VA

10. 3VS/5VS/1.5V (DDR3)

11. 1.05VS/1.5S/1.8V/1.5VA

12. Power Latch/1.5VS/SCREW HOLE

13. CPU Core Power

14. GPU Core Power

15. Penryn Processor(1/2)

16. Penryn Processor(2/2)

17. CPU Thermal

18. Cantiga Host(1/6)

19. Cantiga DMI/Graph(2/6)

20. Cantiga DDRII(3/6)

21. Cantiga Power(4/6)

22. Cantiga Power(5/6)

23. Cantiga Ground(6/6)
24. Clock Generator

25. DDR3 SDRAM SO-DIMM0

26. DDR3 SDRAM SO-DIMM1

27. ICH9M CPU/IDE/SATA(1/4)

28. ICH9M PCI/PCIE/DMI/USB(2/4)

29. ICH9M GPIO(3/4)

30. ICH9M Power/GND(4/4)

31. LCD CNN/SATA/3G/WLAN

32. KBC ITE8512F

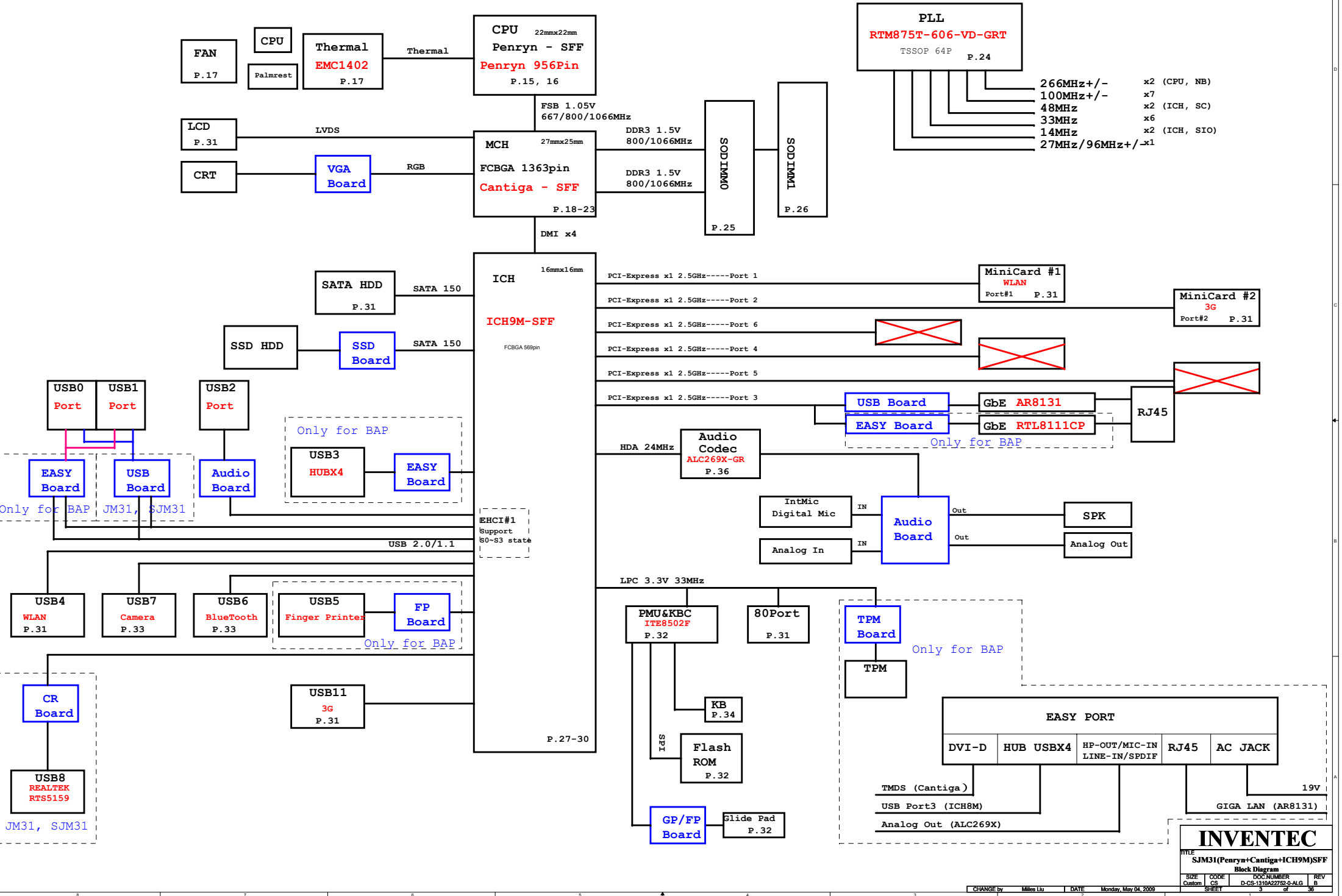
33. IO CN 1/3

34. IO CN 2/3

35. IO CN 3/3

36. Audio Codec

3. Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R

VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI/PCIE/DDRIII DLLs for GMCH/Core/PCIE for ICH9m by SLP_S3#_3R

+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

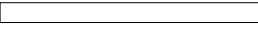



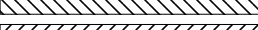



C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	18A
1.05VS	Penryn SFF : AGTL+ termination Cantiga GS: Core Cantiga GS: PCIE Cantiga GS:Core+IMEL+HSIO Cantiga GS:VCC_GMCH Cantiga GS:VCCA_SM_CK and NCTF Cantiga GS:VCC_DMI Cantiga GS:VCCA_SM Cantiga GS:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn SFF PLL Cantiga GS: QDAC Cantiga GS: LVDS Cantiga GS: TVDAC Cantiga GS: Various PLLS analog supply Cantiga GS: VCC_SM_CK Cantiga GS: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GS: HV CMOS Cantiga GS: VCCS_TV DAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:AR8131 Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A 1A
5VS	Cardreader: RTS5159 Azalia Codec: ALC269 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB	4.75V-5.0V-5.25V 5VA 5VA	1A 2A 1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

INVENTEC

FILE: SJM31(Penryn+Cantiga+ICH9M)SFF

ANNOTATIONS

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22782-0-ALG	8

6.Schematic modify Item and History :

- 2009.0108
- 1. ADD USB P3 for Docking, USB P5 for Finger printer,
 Modify CN5 -----P28
 - 2. Modify CN20 to 50pin-----P33
 - 3. Move PWR_SWIN# from CN14 to CN20
 - 4. ADD TPM module-----P34
- 2009.0109
- 1. ADD DOCK_USB_EN, DOCK_CRT_IN#-----P32,33
- 2009.0112
- 1. Change power item: R490,R291,BAT CNN TH PIN

AX1 to A01 change list

- 1. Change AD_ON circiut for Green adaptor PC. (Page 12)
- 2. Change thermal shut down control by PM_ICH_PWROK from ALL_SYSPWRGD. (Page 17)
- 3. Add PCIE I/F to 3G mini card connector for support EM772 (Page24, Page28, Page31)

A01 to A02 change list (JM31 A02, SJM31 A01)

- 1. Add EC_3VLA soft start circuit --- Change R480 to NU, Add Q28, R378,R738,C374,R299,Q118,R739,C376 (Page 9)
- 2. Add 3VA porotect diode --- Add D35 (Page 9)
- 3. For green adaptor --- Change C419 from 0.1uf to 4.7uF , Add Q120, R744,R742,R743 (Page 8, 12)
- 4. For power consumption --- Change Q37,Q50,Q51 from 6015B0090401 to 6015B0082201, Change Q54,Q38,Q48 from 6015B0086301 to 6015B0089301.(Page 8, 10, 11)
- 5. Change R29,R30,R31,R32,R33,R34,R35 from 0 Ohm to short pad. (Page 13)
- 6. For safty ---- Change R231 from 0 Ohm to 330 Ohm, R226 from 665 Ohm to 330 Ohm. (Page 27)
- 7.For 3G leakage ---- Delete R220,R211 (Page 29)
- 8. Delete reverse HW timing circuit. ---- Delete U7,D13,R237,C376,U9,U8,D9,R222,C327 (Page 29, 32)

A02 for SJM31 change list

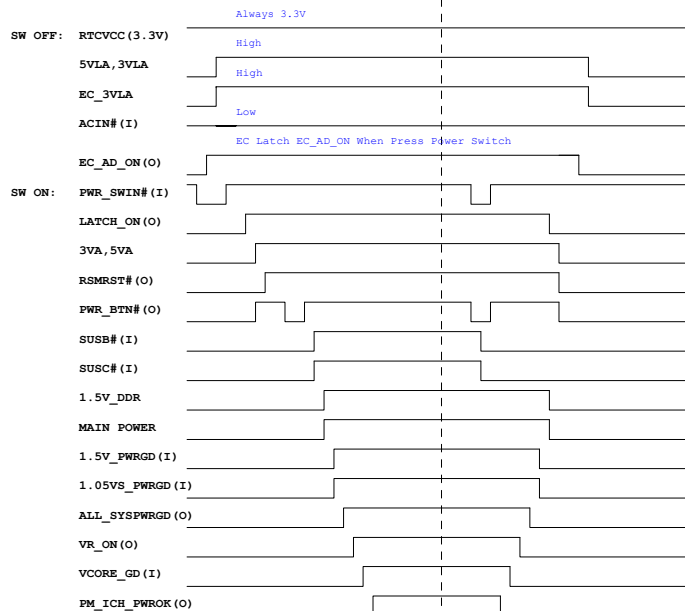
- 1. R513 change to 470 for SJM31 TP lock LED

SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

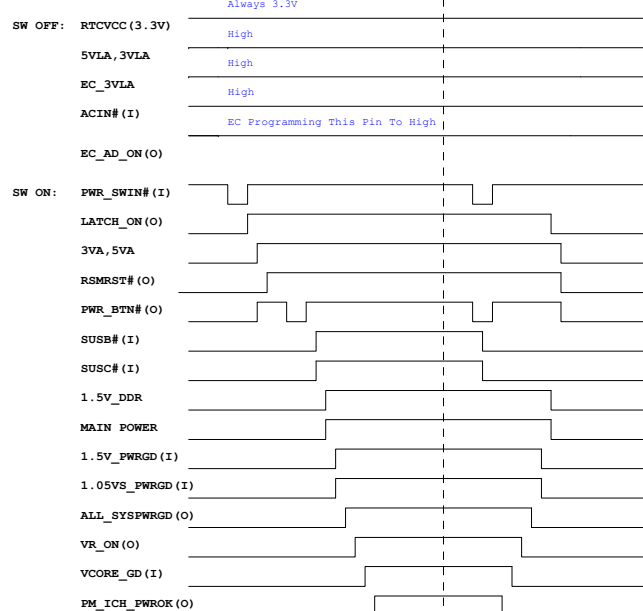
Power on/off sequence AC insert (without Battery Pack)

Power on sequence Power off sequence



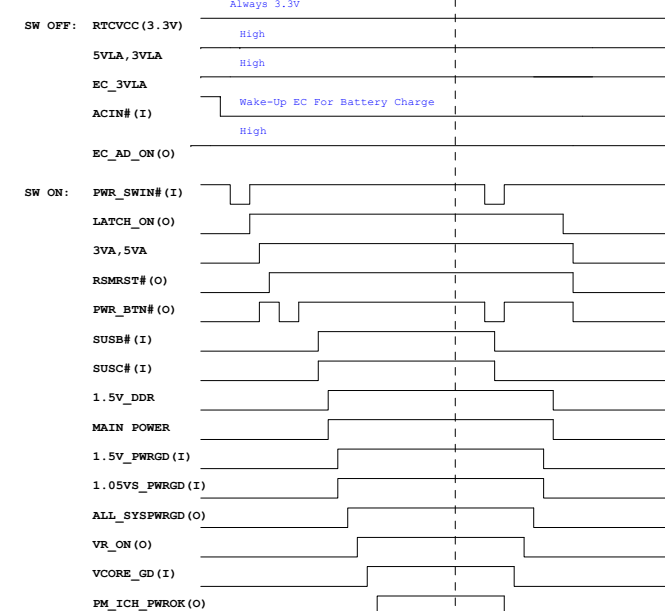
Power on/off sequence Battery insert (without AC adapter)

Power on sequence Power off sequence



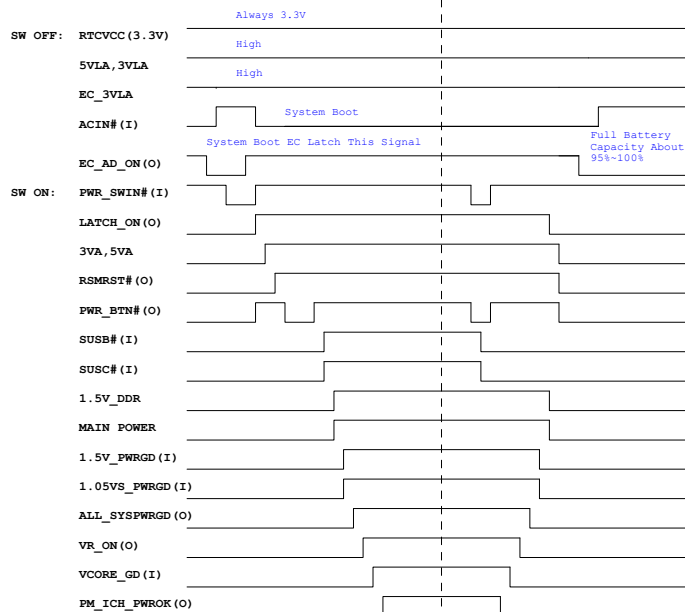
Power on/off sequence AC insert(with charge over 95%)

Power on sequence Power off sequence



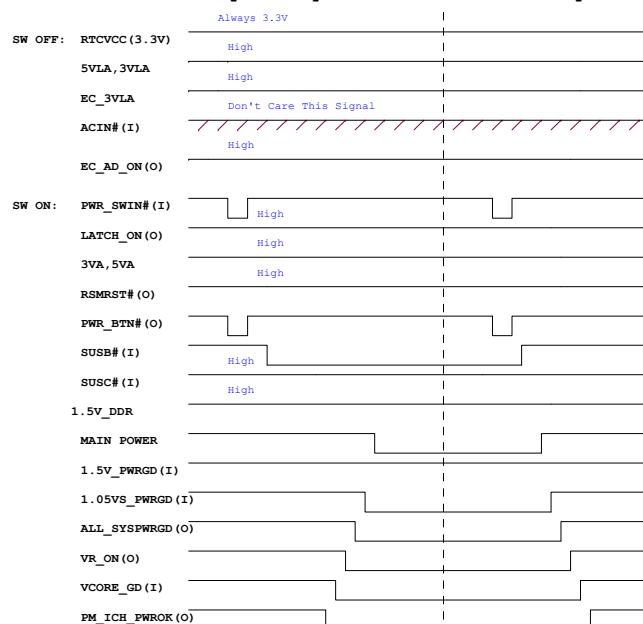
Power on/off sequence AC insert(without charge over 95%)

Power on sequence Power off sequence



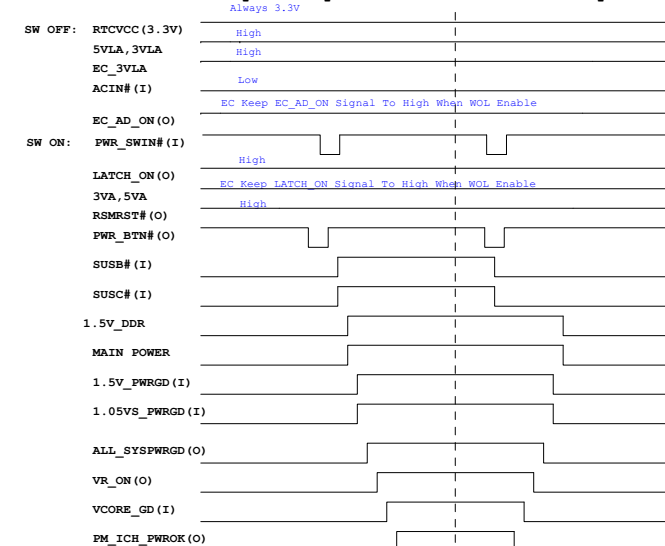
Suspend And Resume Sequence (S3)

Suspend sequence Resume sequence



Power on/off sequence after windows shoutdown (WOL enable)

Suspend sequence Resume sequence



INVENTEC

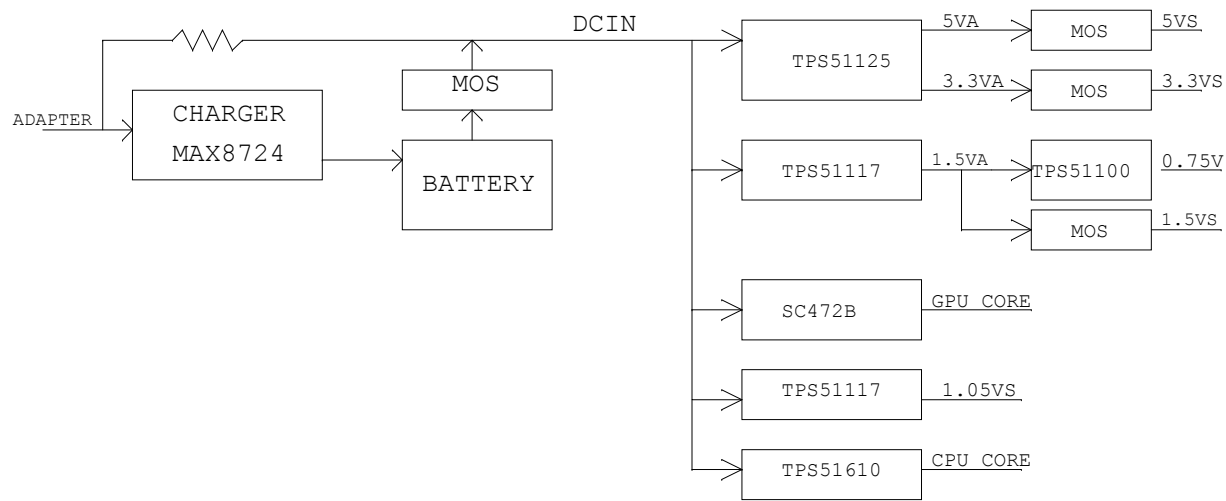
TITLE
SJM31(Penryn+Cantiga+ICH9M)SWF
Time Diagram

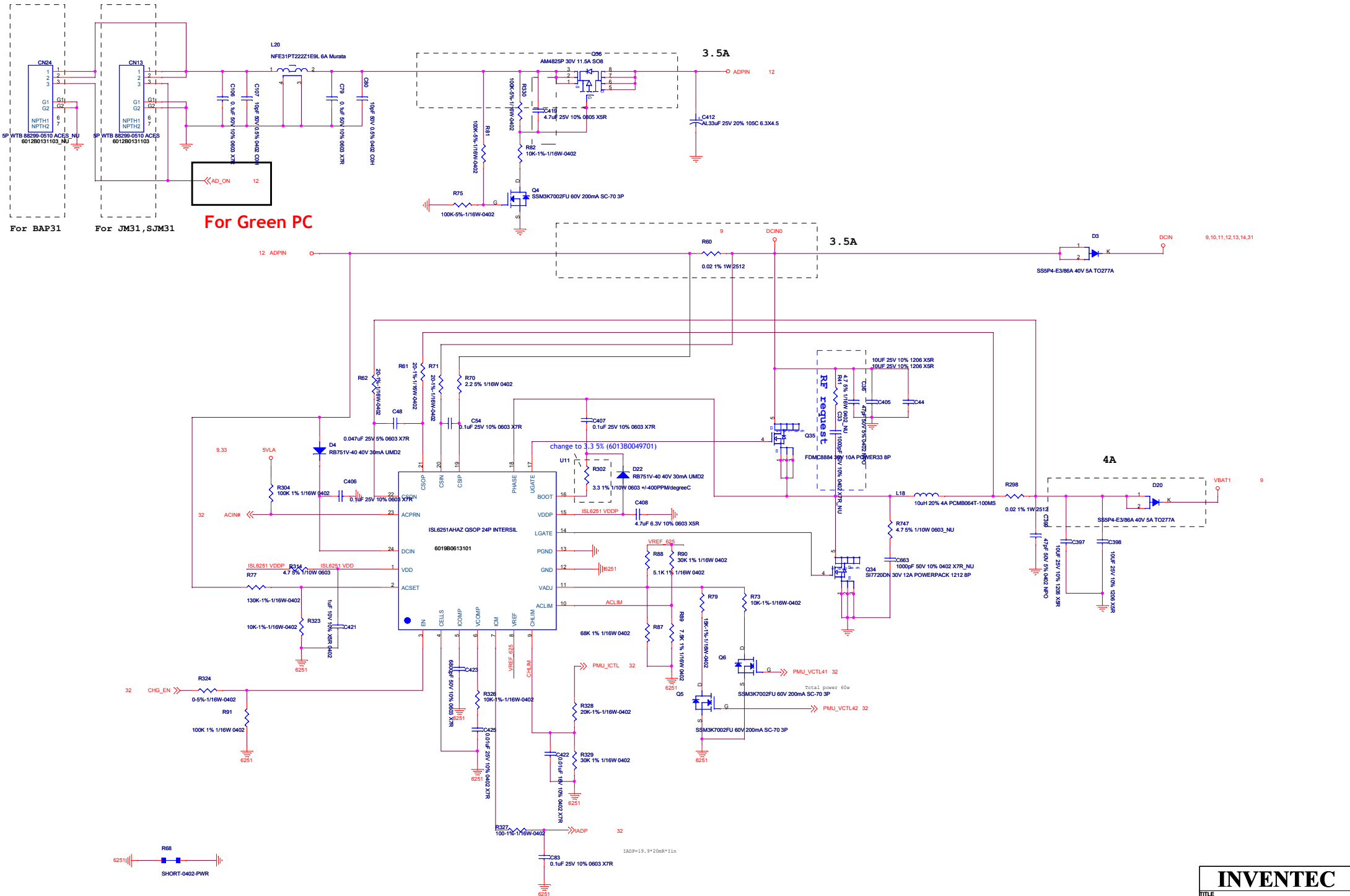
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Custom CS D-CS-1310A2752-0-ALG B

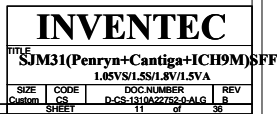
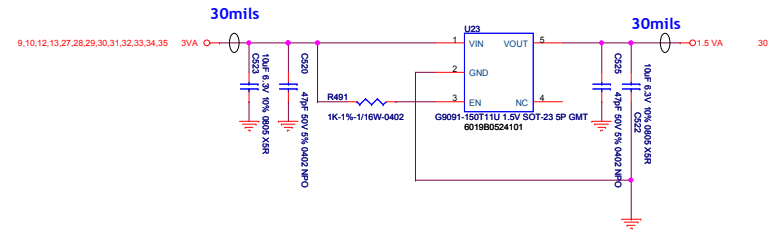
CHANGE by Miles Liu DATE Monday, May 04, 2009

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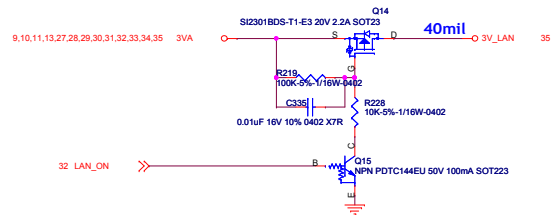
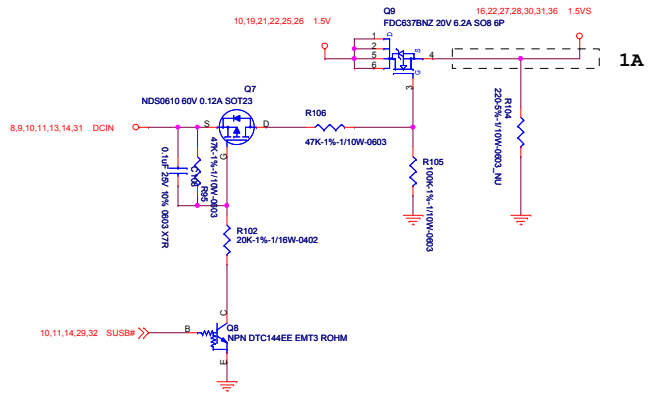
Power Block Diagram :



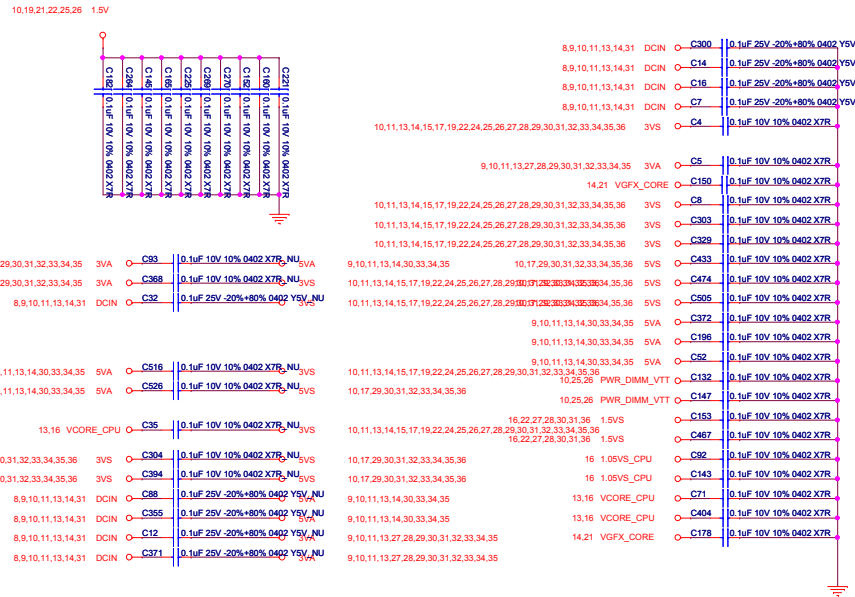




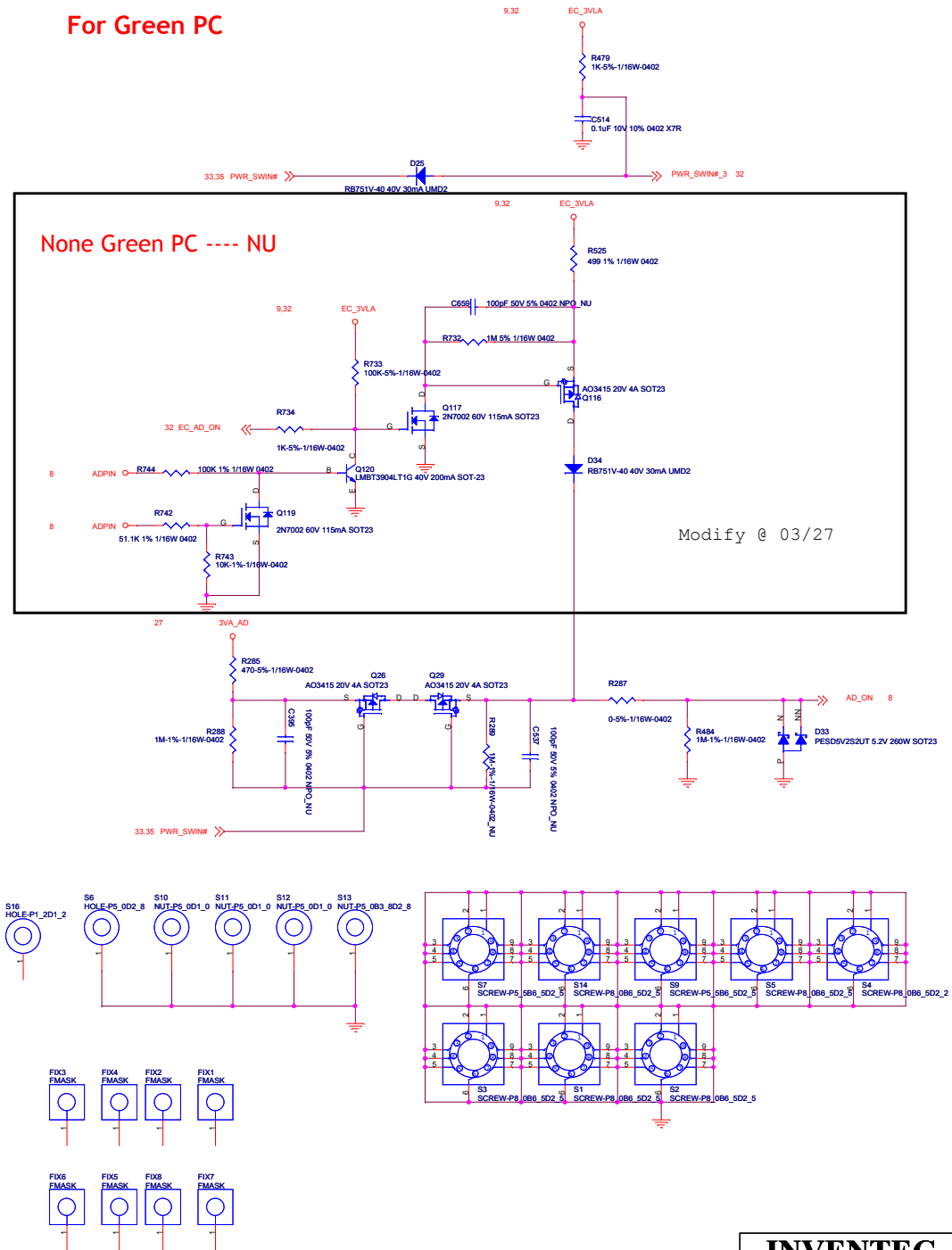
1.5VS



EMI Cap



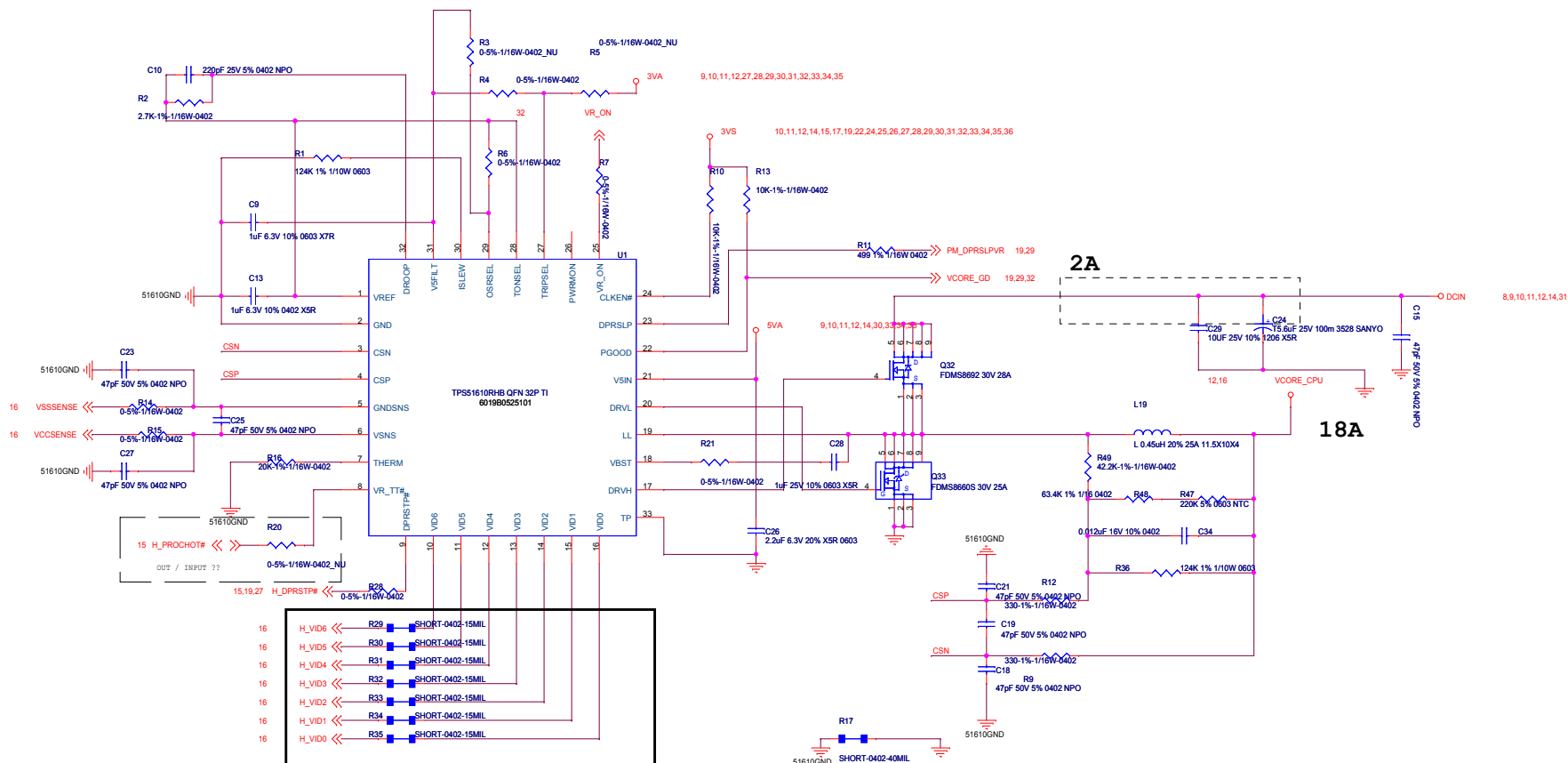
For Green PC

**INVENTEC**

TITLE	SJM31(Penryn+Cantiga+ICH9M)\$FF
	Power on latch

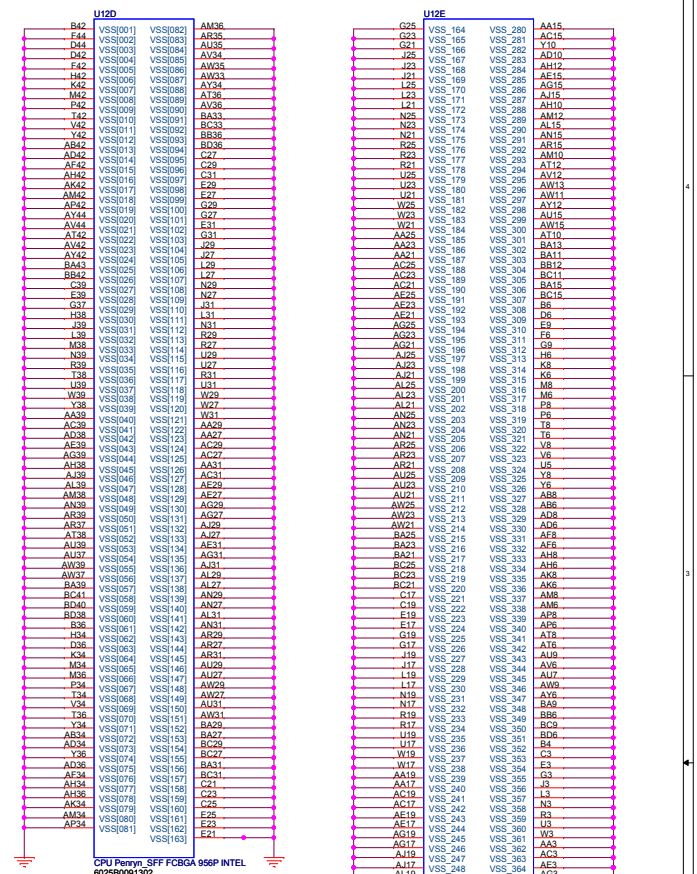
SIZE Custom	CODE CS	DOC.NUMBER D-CS-1310A22752-0-ALG	REV B
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CHANGE by	Miles Liu	DATE	Monday, May 04, 2009
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16 H_VID6 << R29 SHORT-0402-15MIL
 16 H_VID5 << R30 SHORT-0402-15MIL
 16 H_VID4 << R31 SHORT-0402-15MIL
 16 H_VID3 << R32 SHORT-0402-15MIL
 16 H_VID2 << R33 SHORT-0402-15MIL
 16 H_VID1 << R34 SHORT-0402-15MIL
 16 H_VID0 << R35 SHORT-0402-15MIL
 16 H_VID0 << R36 SHORT-0402-40MIL

Modify to short pad@ 03/27

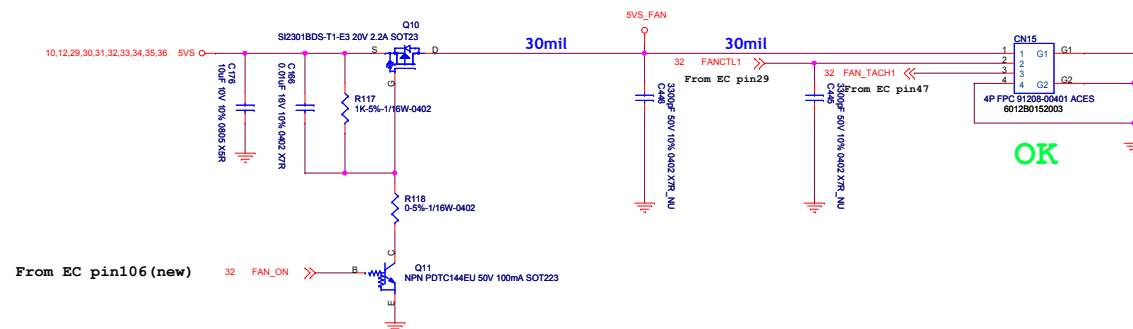
[illegible]

Comp0,2 connect with $Z_0=27.4\text{ohm}$, make trace length shorter than 0.5" and width is 18mils.
Comp1,3 connect with $Z_0=55\text{ohm}$, make trace length shorter than 0.5" and width is 5mils

THERMAL SENSOR



Fan control

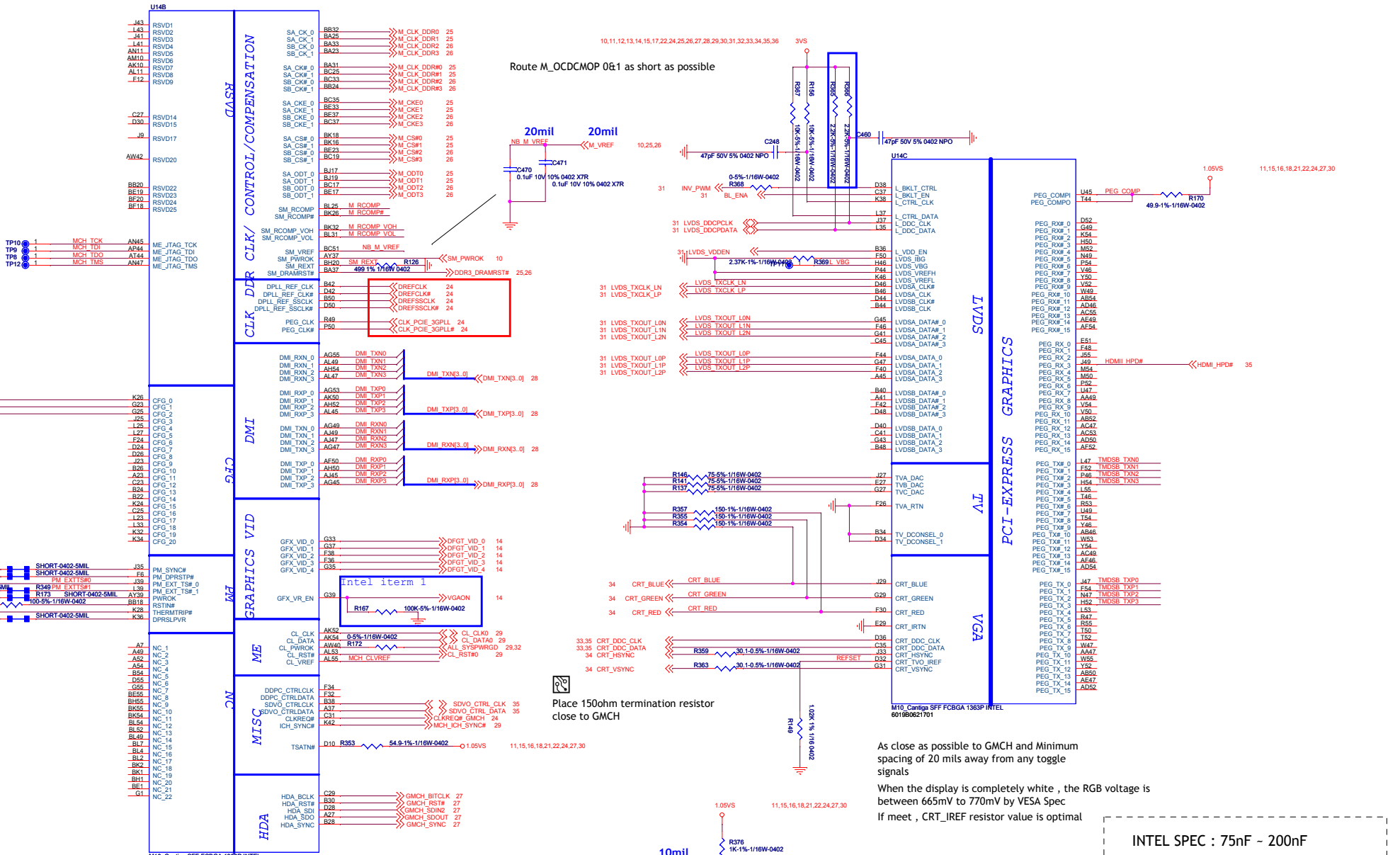


OK

INVENTEC

TITLE	SJM31(Penryn+Cantiga+ICH9M)SFF
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CPU Thermal			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B
SHEET		17	of 36



Cantiga Strapping:		
	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(I7PM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIe Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIe loopback)	Enable	Disable(default)
MCH_CFG12 (ALL2)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIe x1 is operation	Only SDVO or PCIe x1 with PEG port

INTEL SPEC : 75nF - 200nF			
TMDSB_TXN0	C291	0.1uF 10V 10% 0402 X7R	TMDSB_TXN0 35
TMDSB_TXP0	C290	0.1uF 10V 10% 0402 X7R	TMDSB_TXP0 35
TMDSB_TXN1	C293	0.1uF 10V 10% 0402 X7R	TMDSB_TXN1 35
TMDSB_TXP1	C292	0.1uF 10V 10% 0402 X7R	TMDSB_TXP1 35
TMDSB_TXN2	C294	0.1uF 10V 10% 0402 X7R	TMDSB_TXN2 35
TMDSB_TXP2	C295	0.1uF 10V 10% 0402 X7R	TMDSB_TXP2 35
TMDSB_TXN3	C297	0.1uF 10V 10% 0402 X7R	TMDSB_TXN3 35
TMDSB_TXP3	C296	0.1uF 10V 10% 0402 X7R	TMDSB_TXP3 35

INVENTEC

FILE
SJM31(Penryn+Cantiga+ICH9M)SFF

Cantiga DMI/Graph2(6)

SIZE
Custom

CODE
CS

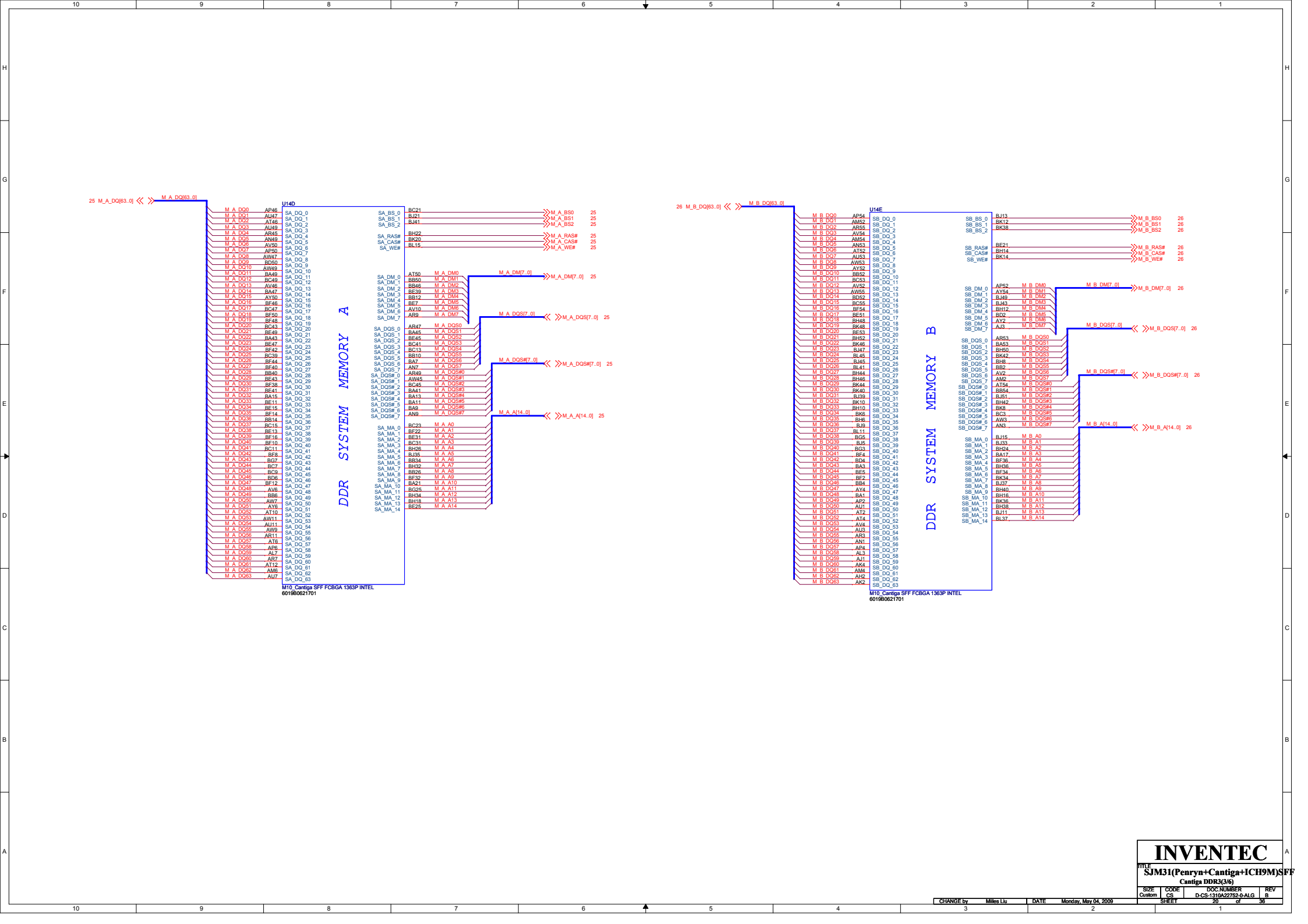
SHEET
19

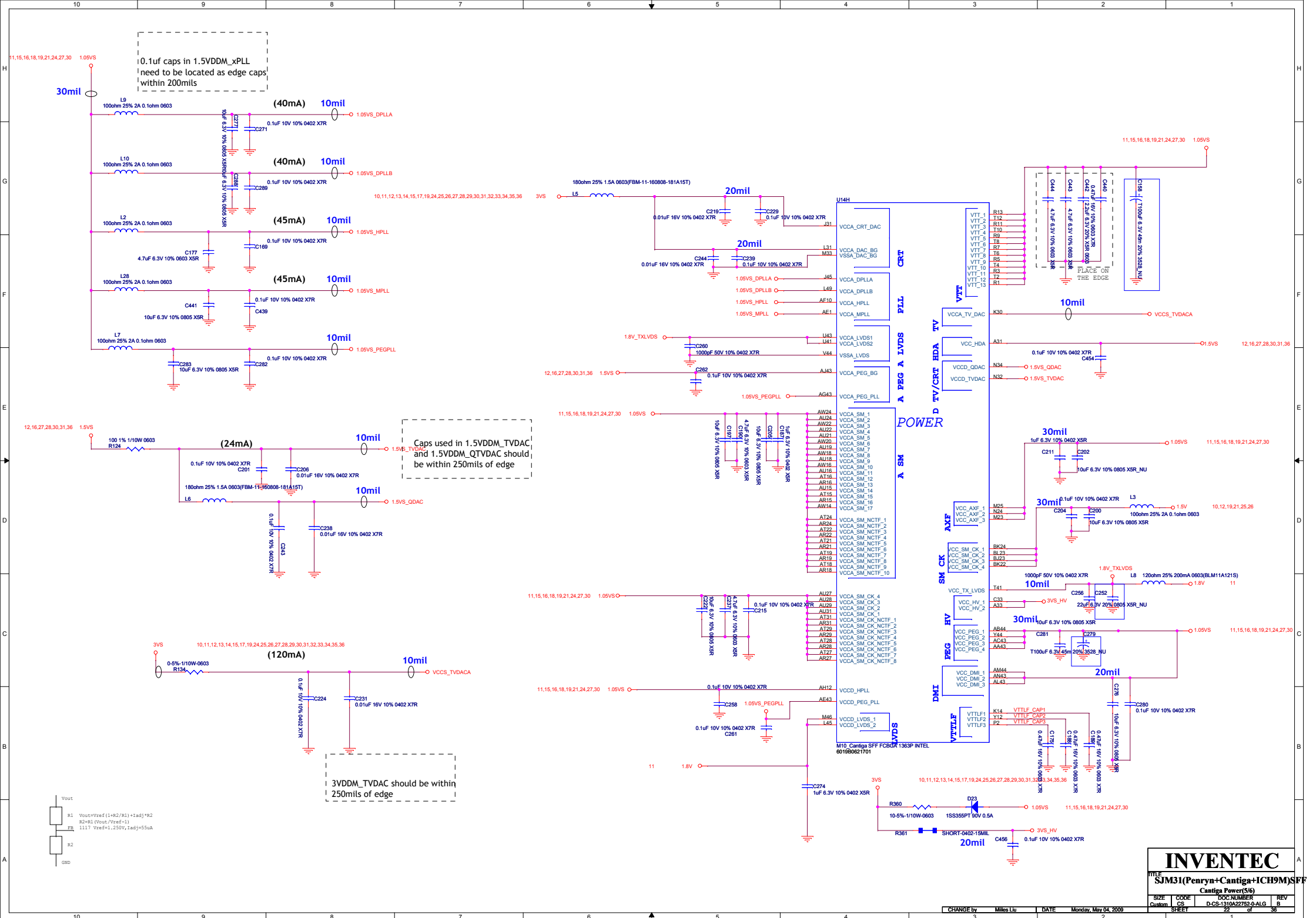
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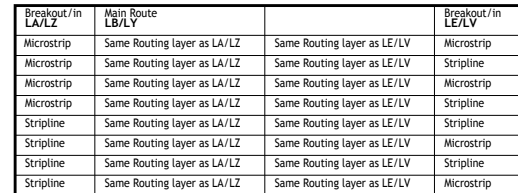
REV
B

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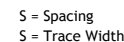
CHANGE by Miles Liu DATE Monday, May 04, 2009





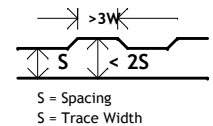
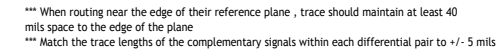


*** Match the trace lengths of the complementary signals within each differential pair to ± 5 mils

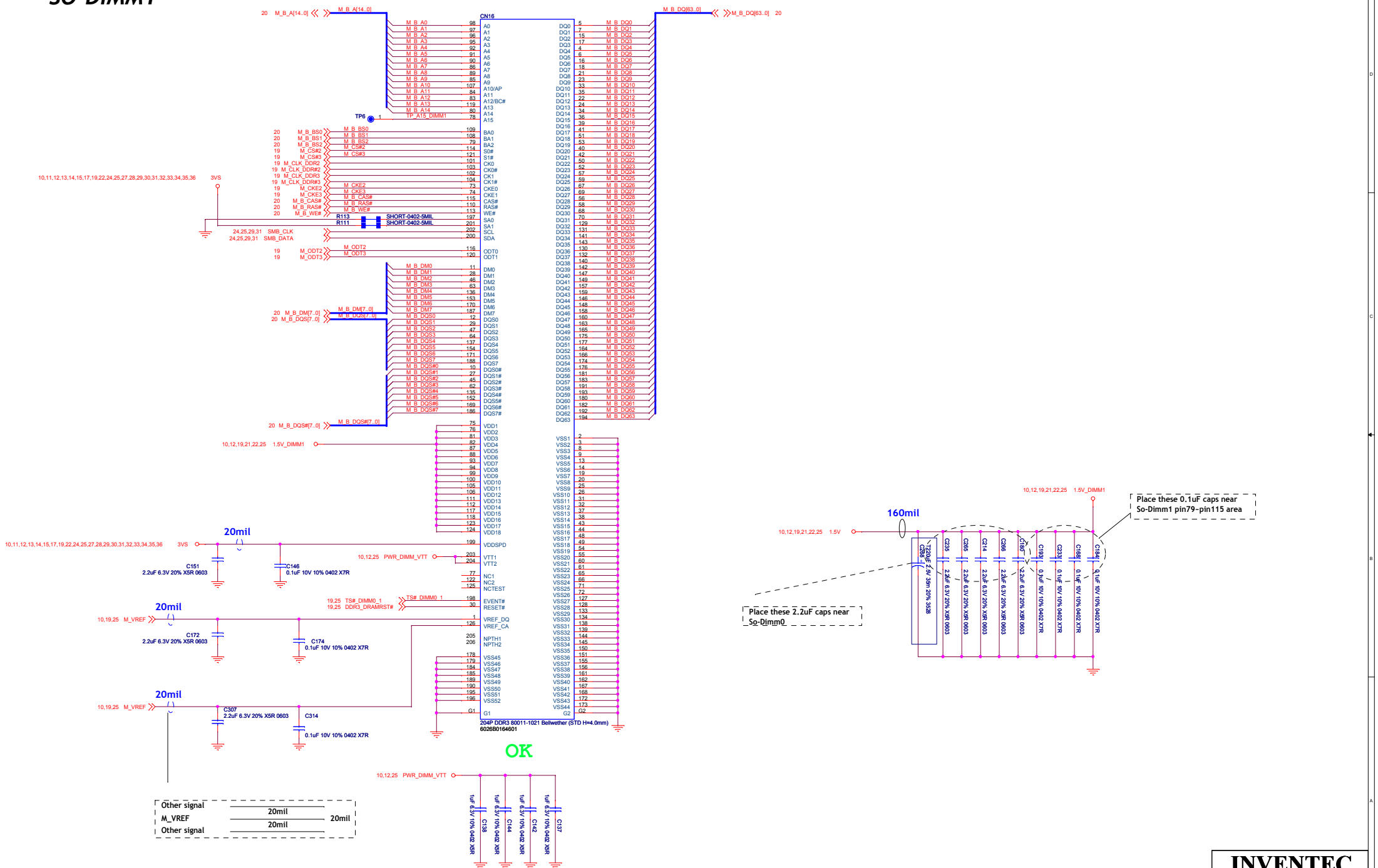


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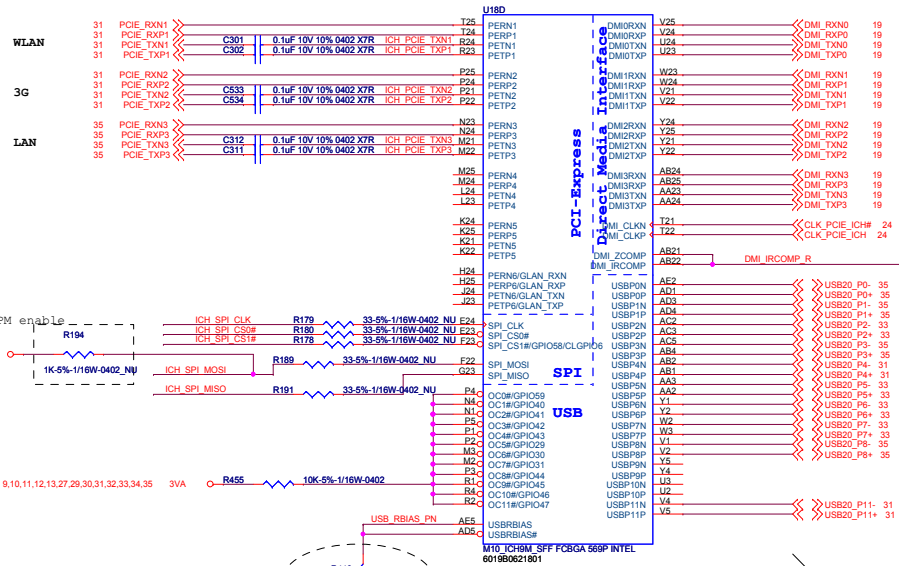
graph LR
    subgraph GMCH
        Tx1[Tx]
        Rx1[Rx]
    end
    subgraph ExpressMiniCard [Express/Mini Card]
        Rx2[Rx]
        Tx2[Tx]
    end
    Tx1 --- LA
    LA --- LB
    LB --- LC
    LC --- Rx2
    Rx1 --- LZ
    LZ --- LY
    LY --- Tx2
    style LB stroke-dasharray: 5 5
    style LC stroke-dasharray: 5 5
  
```



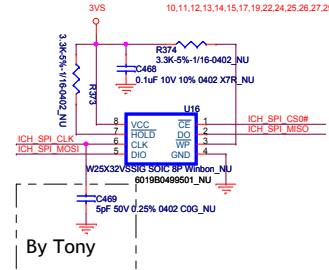
SO-DIMM 1



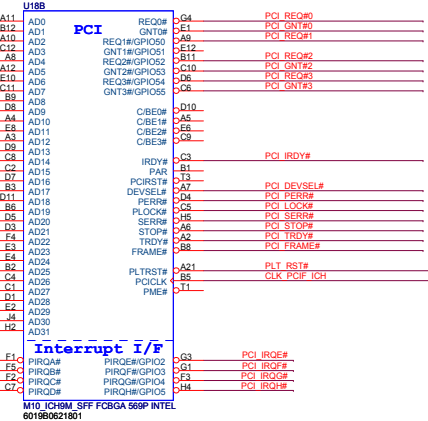
PCIe AC coupling caps need to be within 250mils of the driver



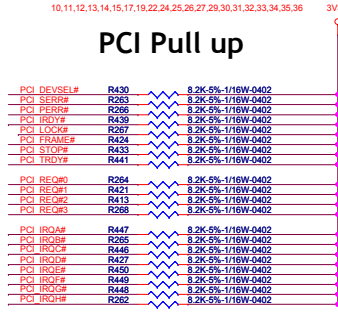
Place within 500mils of ICH



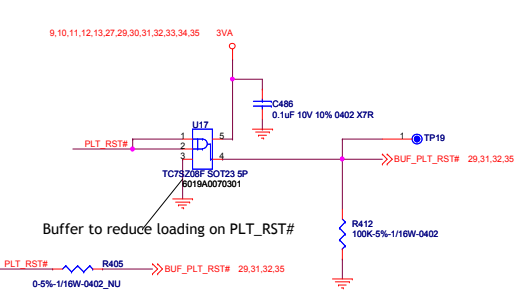
By Tony



M10 ICH9M SFF FCBGA 568P INTEL 6019B0021801



PCI Pull up



PCI_GNT#3 No stuff: by default Stuff: For A16 swap override

PCI_GNT#0	SPL_CS#1	
1	1	LPC
1	0	PCI
0	1	SPI

Check BIOS type

[illegible]

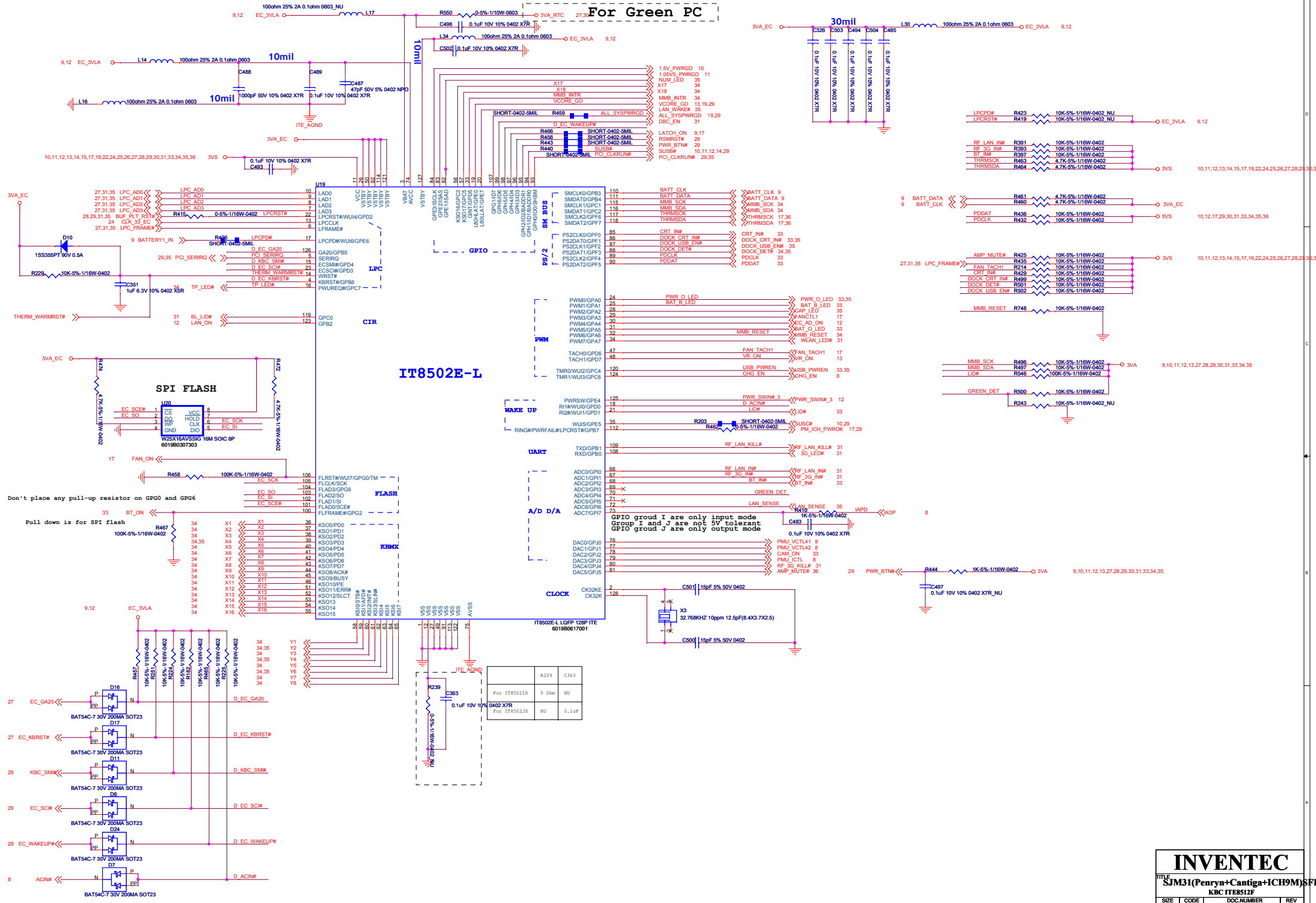
LCD brightness control

[illegible]

INVENTEC

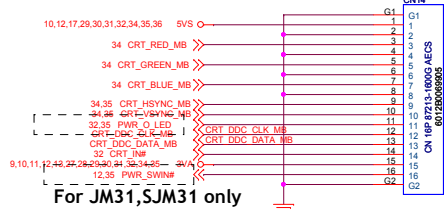
TITLE
SJM31(Penryn+Cantiga+ICH9M)SFF
LCD CNN & WLAN & 3G

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22752-0-ALG	B

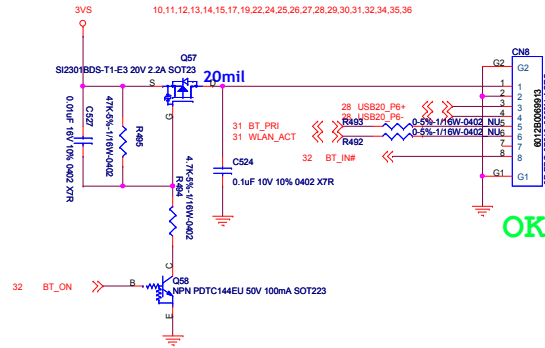


VGA Board CN

(CRT+ PWR SW)

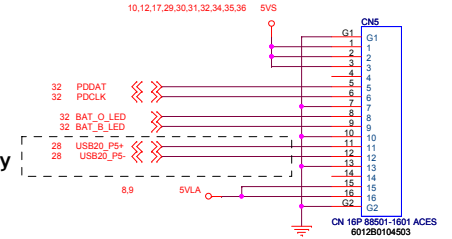


Bluetooth CON.

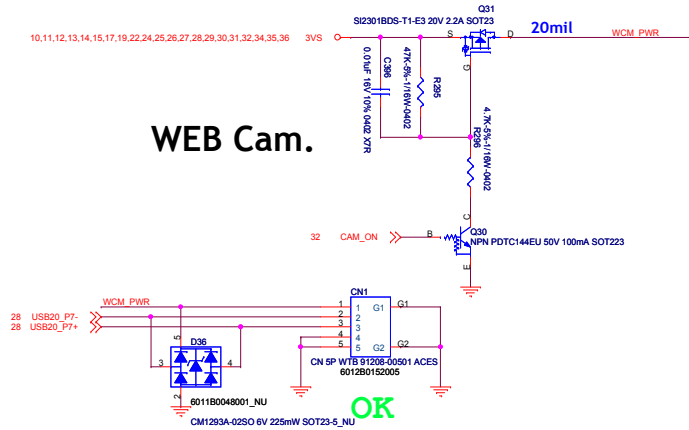


GLIDE PAD Board

For BAP31 only

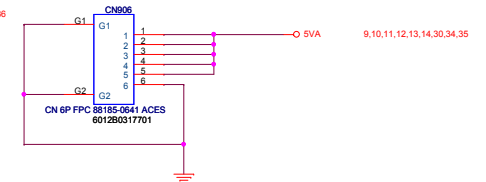
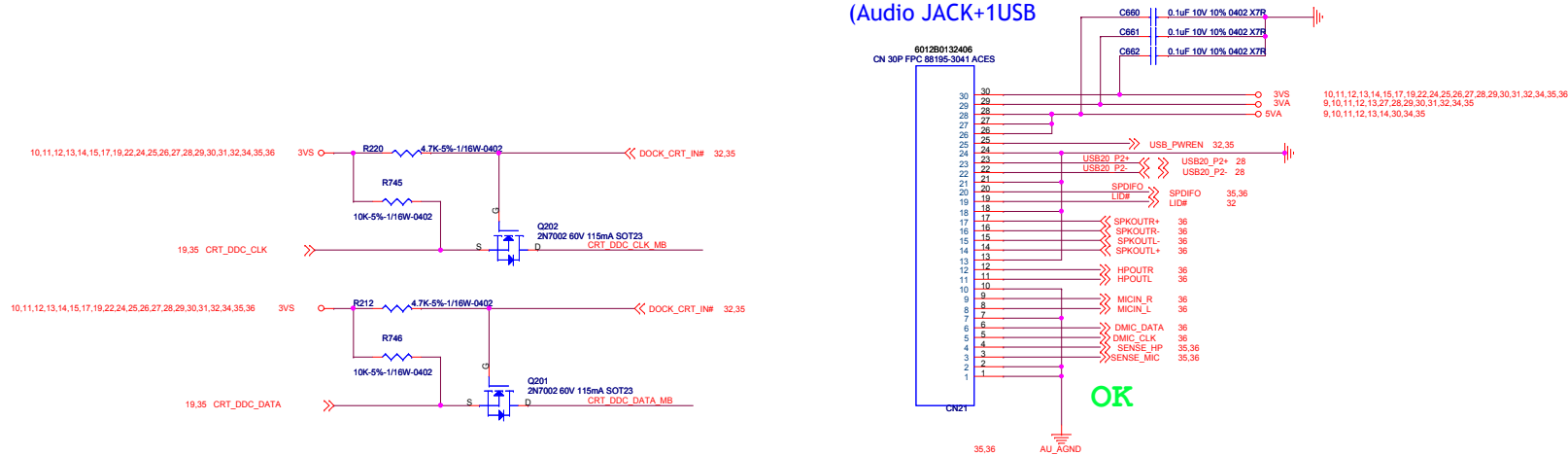


WEB Cam.



AUDIO Board CN

(Audio JACK+1USB)



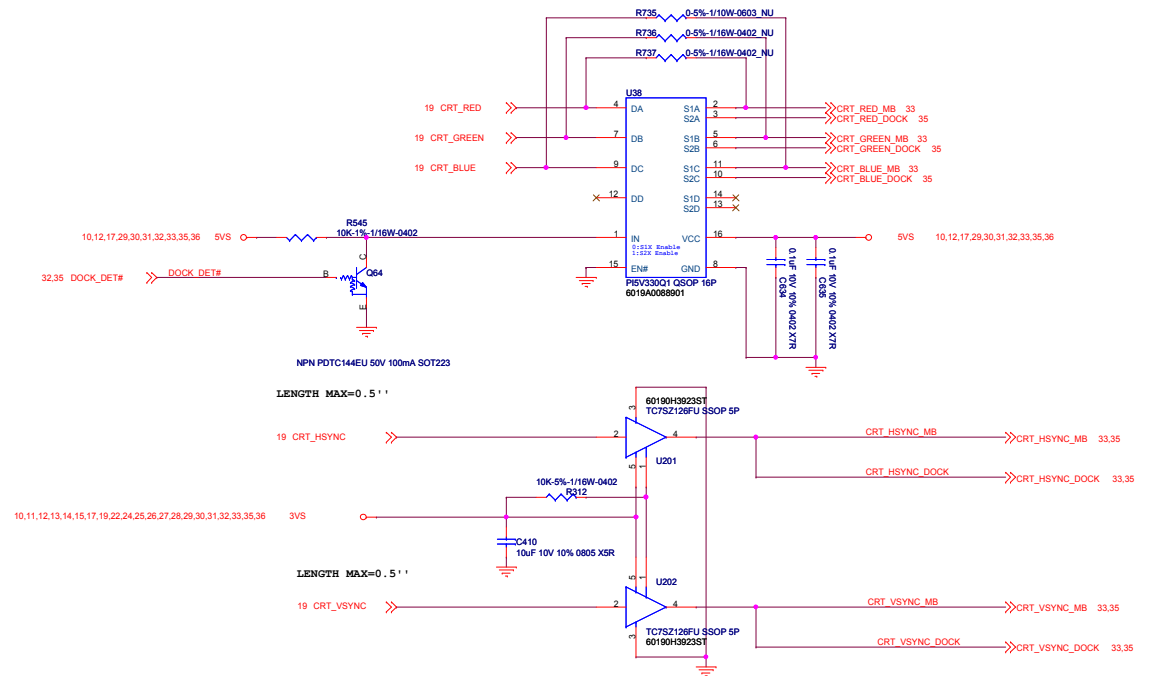
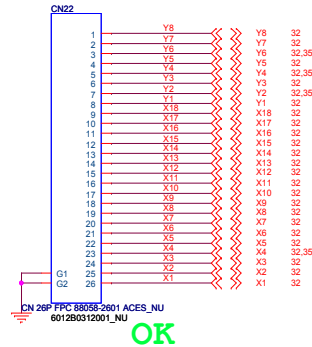
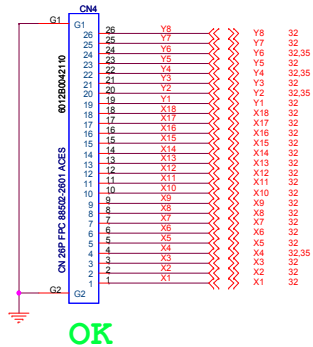
INVENTEC

TITLE			
SJM31(Penryn+Cantiga+ICH9M)SFF			
Daughter Connector			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A22732-0-ALG	B
SHEET			
33	34	35	36

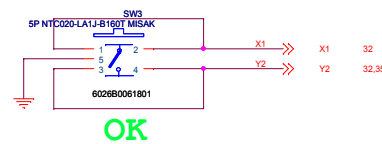
CHANGE by Milos Liu DATE Monday, May 04, 2009

To K/B(For JM31,BAP31)

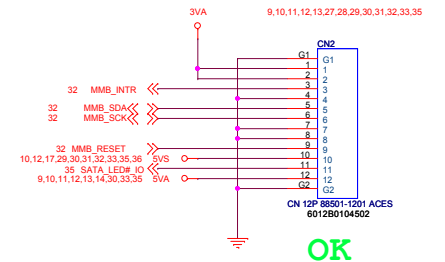
To K/B (For SJM31)



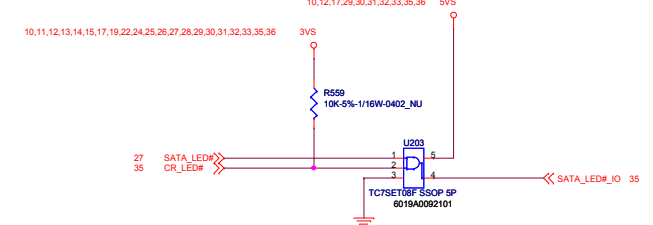
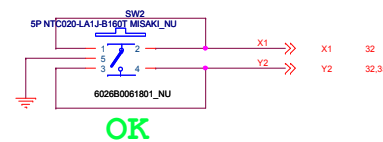
SW (FOR SJM31)



SW Sensor BOARD(For JM31,SJM31)



SW (FOR JM31,BAP31)



GP lock Button / LED(FOR SJM31)

JM31 ---- 120 Ohm
SJM31 ---- 470 Ohm

GP lock Button / LED(FOR BAP31)

GP lock Button / LED(FOR JM31)

